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3-D Bonding by Solid - Liquid Interdiffusion

George Riley
FlipChips Dot Com

A recent 3-D technology survey paper from Fraunhofer IZM [1] reports their progress in 3-D chip-to-wafer stacking with inter-chip vias and solid-liquid interdiffusion bonding (SLID). This approach is an example of the next-generation bonding techniques being developed in the race for commercially-viable heterogeneous integrated systems.

After wafer-level processing, testing, thinning, and separation, known good die are bonded face-up to known good die on the bottom wafer. Figure 1 shows a cross-section schematic of multiple die stacking with this technique.

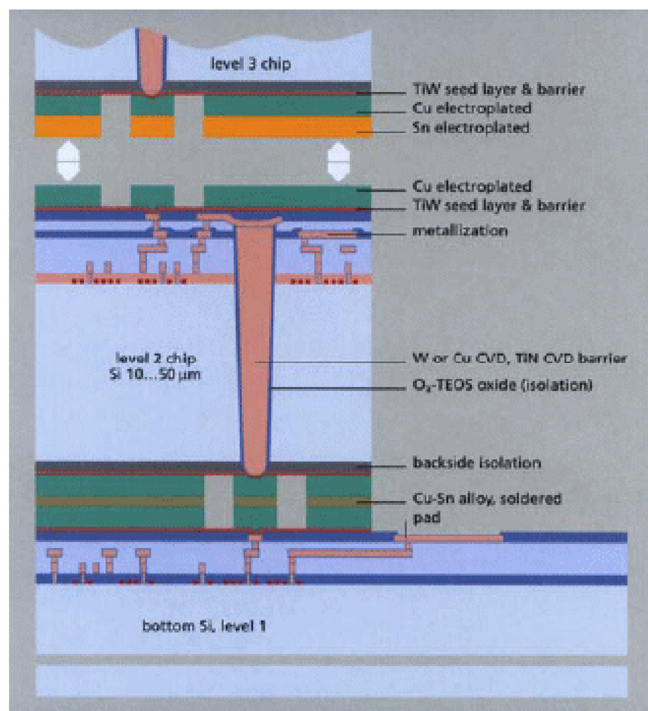

Figure 1. Diagram of vertical integration with SLID bonding.

The top wafer processing includes creating tungsten-filled vias of 1 to 3 µm diameter. Wafer thinning exposes the vias.

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Electroplating masked-defined tin/copper provides a contact layer after completing dielectric deposition and via opening.

Contacts are defined in the tin/copper layer, and non-contact areas remain as deposited for stronger mechanical bonding of the die to the wafer.

The top surface of the bottom wafer is electroplated with copper masked to match the top wafer.

The tested and diced top-wafer chips are aligned and placed onto the bottom wafer for joining.

Soldering under pressure at 300 ºC causes the liquid tin to become interdiffused with copper, creating a copper-tin intermetallic, Cu_3Sn. This intermetallic is stable, with a melting point of 600 ºC.

The tin is rapidly consumed, leaving both sides with copper layers.

Figure 2 shows a cross-section of SLID interconnected devices in a test structure. The tungsten-filled vias are connected to the aluminum tracks on the top device, and connected through the Cu/Sn system to the bottom device.

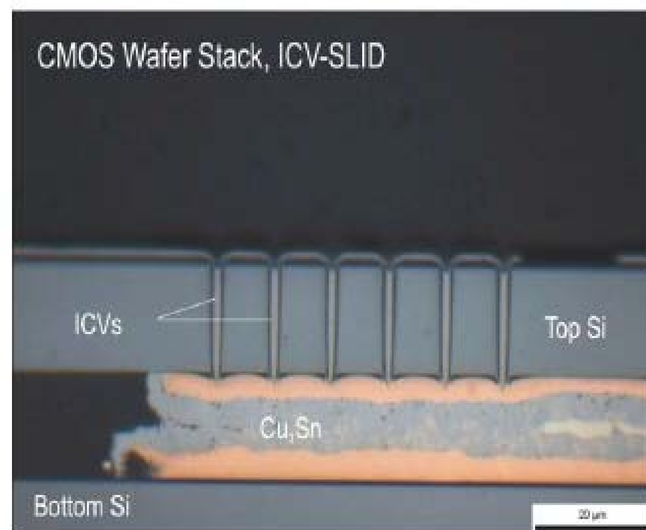

Figure 2. Cross-section view of completed SLID connections.

The paper concludes that the TSV - SLID technology will support a new generation of device stacking with interconnection densities in the range of 10^4 to 10^6 per square centimeter.

FOR MORE INFORMATION

A broad survey of integration technologies, with technical details, illustrations, and citations may be found in:

"Technologies for 3D Heterogeneous Integration,"

M. Jurgen Wolf, wolf@izm.fraunhofer.de

Peter Ramm, ramm@izm.fraunhofer.de

Herbert Reichl, reichl@izm.fraunhofer.de

Proceedings of SMTA Pan Pacific Symposium 2008.

The paper is available from SMTA in the Knowledge Base at www.SMTA.org.

FlipChips Dot Com
210 Park Ave #300
Worcester, MA 01609 USA
Phone 508-753-3572
FAX 508-757-0220
EMAIL DrRiley at flipchips.com

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