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## Transfer Printing

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Transfer printing, an emerging technology being commercialized by Semprius, is the assembly equivalent of simultaneously picking and placing thousands of die directly from a semiconductor wafer onto almost any kind of substrate.

### Process

The massively parallel printer employs a patterned, microstructured elastomeric stamp to lift a selected array of die from a pre-treated wafer and place them accurately on the substrate.

The source wafer, which may be silicon or other high performance semiconductors, is prepared through a sacrificial layer process common to MEMS fabrication. For example, silicon devices may first be fabricated upon SOI (silicon-on-insulator) wafers having a buried oxide layer. The finished die are made releasable by etching through the silicon to the oxide layer, which is then removed by a selective wet etchant.

Although freed from the underlying wafer, the die are held in place by microfabricated "tethers" that break upon device pickup by the stamp.

In assembly, the transfer stamp is aligned above the wafer, brought into contact with the selected die, and lifts them away from the wafer. The stamp then moves into alignment over the substrate and deposits the devices.

The devices are peeled from the stamp by lifting it at a different rate than used when picking up devices. The stamp returns to the wafer and repeats the transfer cycle.

### Illustration

Figure 1, from the cited paper that Semprius presented at SMTA International 2008, shows the sequence:

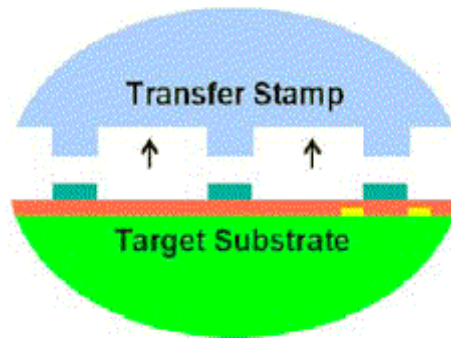


Figure 1a. The transfer stamp is aligned over the source wafer and the pattern of protruding elastomeric posts is brought down to contact the selected die.

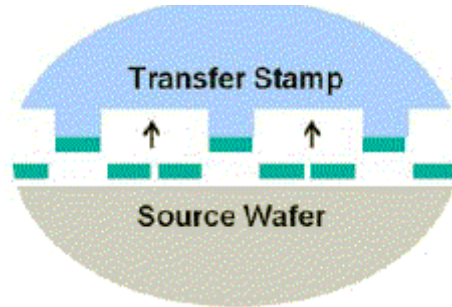


Figure 1b. The transfer stamp is lifted at a controlled rate to break the tethers and remove the selected die from the wafer.

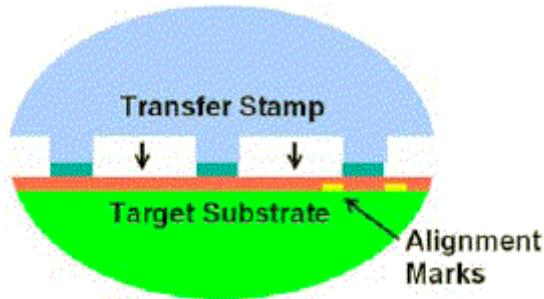


Figure 1c. The transfer stamp is aligned above the substrate and lowered to place the die onto the surface.

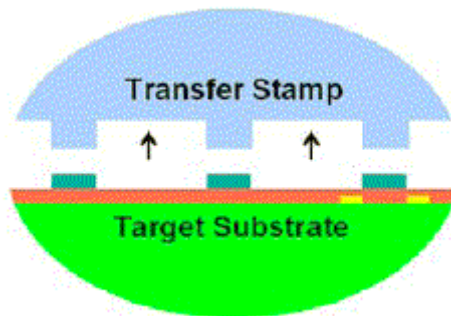


Figure 1d. The transfer stamp is lifted at a controlled rate different from the pickup rate, leaving the die in position on the substrate.

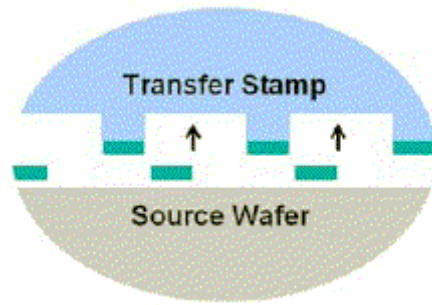


Figure 1e. The transfer stamp moves to the source wafer and steps into alignment with the next group of die to be transferred.

### Advantages

- **High Transfer Rate** – the stamp can simultaneously place thousands of die in a cycle time of less than one minute.
- **High Assembly Rate** – assuming only one transfer cycle per minute, the printer could transfer about 170,000 die per hour. An anticipated future cycle time of 20 seconds would transfer about 1 million die per hour.
- **High Yield** – Semprius has demonstrated yields of 100% in transferring 2,850 chips with dimensions 450  $\mu\text{m}$  by 40  $\mu\text{m}$  by 5  $\mu\text{m}$  to a silicon target wafer and to a flexible plastic target sheet
- **High Accuracy** – Semprius has demonstrated a placement accuracy measured at  $\pm 4 \mu\text{m}$ .
- **Wide Substrate Range** – because wafer processing is separated from substrate attachment, a wide range of substrate materials can be used without limiting the semiconductor devices or processes.
- **Pitch Magnification** – since the picked devices need not be adjacent on the source wafer, spacing the pickup posts at some multiple of die pitch allows a wider range of die spacing on the substrate.
- **Form Factor Independent** – the transfer stamp approach easily accommodates die form factors of 10X or higher, difficult for pick-and-place equipment to handle.
- **Small Die** – standard pick-and-place vacuum collets do not easily handle device dimensions below 100  $\mu\text{m}$  or die thinner than 20  $\mu\text{m}$ . Transfer printing has demonstrated high-accuracy high-yield placement of 5  $\mu\text{m}$  thick die.

### Applications

Semprius has identified potential applications including glass or plastic display or sensor backplanes, flat panel X-ray detector backplanes, solar cell photovoltaics, and advanced semiconductor packaging.

### FOR MORE INFORMATION

"Transfer Printing: An Emerging Technology for Massively Parallel Assembly of Microdevices," by C.A. Bower, E. Menard, & P.E. Garrou

