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Laminated Chip Packages

George Riley, FlipChips Dot Com

The continuing drive towards increased miniaturization and multilayer stacking has stimulated renewed interest in embedding die into substrates. Embedding supports multilayer stacking, creates short, well-controlled interconnections, and protects the chip.

Since the mid-nineties, General Electric has been the pioneer of embedded die with their "Chips First" approach. They see their current "Embedded Chip Build Up" (ECBU) solderless process as an attractive alternative to fine pitch flip chip.

Now others are introducing different methods to meet differing electrical and mechanical needs. For example, Fraunhofer IZM recently announced progress with their laminated embedded die "Chip in Polymer" packaging, based upon standard circuit board equipment and techniques.

Figures 1a - 1e show the steps in the IZM process. Prior preparation includes a suitable organic or inorganic core substrate, and wafer preparation of the die bond pads. Die are then bonded to the substrate, laminated with a dielectric, and linked to the external circuitry.

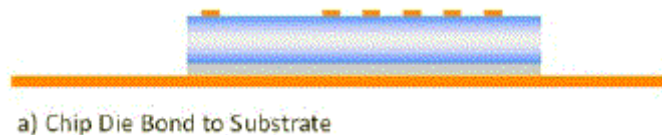


Figure 1a depicts bonding thin die to the substrate, in a pads-up position. Placement accuracy is $\pm 10\mu\text{m}$. Bonding may be by dispensed or screen-printed adhesives, or by die attach film. The die film advantage is better coplanarity and adhesive thickness control.

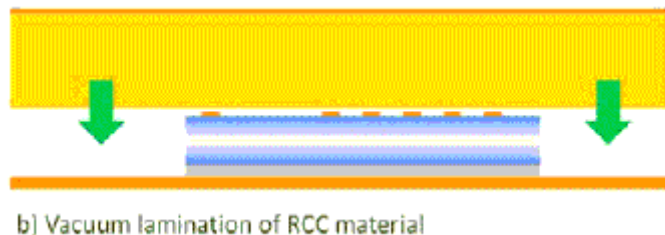
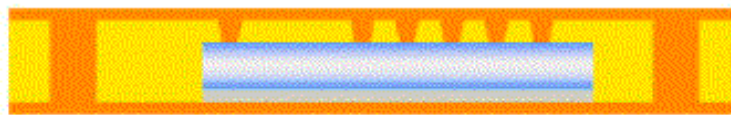


Figure 1b Lamination. The preferred dielectric is resin-coated copper (RCC), providing both dielectric and a copper layer for later interconnections. Vacuum lamination, a standard PCB operation, assures a uniform, void-free dielectric layer.



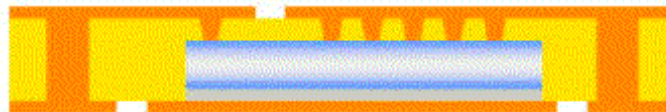
c) Laser drilling of micro via

Figure 1c Via Drilling. Laser drilling of the RCC creates vias to the chip bond pads and to the substrate. A single UV laser can drill through the copper layer and the dielectric. Alternatively, a UV laser for the copper layer followed by a CO₂ laser ablating the dielectric permits faster drilling without risking damage to the bond pads, which are immune to CO₂.



d) Copper metallization

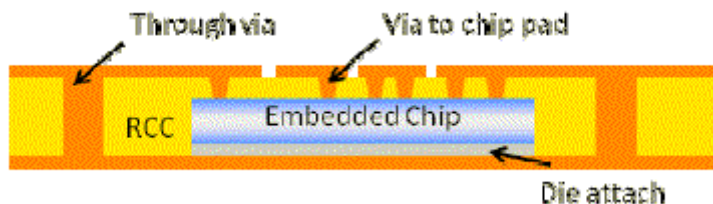
Figure 1d Metallization. Copper deposition in the vias requires a multi-step procedure. A cleaning step removes organic debris and roughens the dielectric surface to improve adhesion. Depositing a conductive colloid on the epoxy surface permits metallizing the vias. Deposited electrolytic copper forms the via connections.



e) Structuring of conductor lines

Figure 1e Interconnection. Circuit interconnections in the copper metal layer may be formed by etching or laser direct structuring. A subtractive etch with tin masking removes unwanted copper. Alternatively, laser patterning allows finer-pitch structures.

Figure 2 is a cross-section drawing of the completed package. Wafer sawing or laser cutting separates the packaged devices.



In summary, multiple layers of laminated thinned die provide an alternative route to high-density 3D interconnection that does not depend on high precision wafer alterations such as through-silicon vias (TSV).

FOR MORE INFORMATION

Lars Boettcher et. al., "Embedded Packages – Technology and Applications,"
Proceedings of the 2008 SMTA International Symposium, Session ET-1, August
2008, available from [SMTA](#)

For more information, visit the Fraunhofer Institute for Reliability and Microintegration
(IZM) web site at [IZM](#)

FlipChips Dot Com
210 Park Ave #300
Worcester, MA 01609 USA

Phone 508-753-3572
FAX 508-757-0220
EMAIL DrRiley at flipchips.com

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