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Tutorial 86 - - September 2008

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George Riley, FlipChips Dot Com

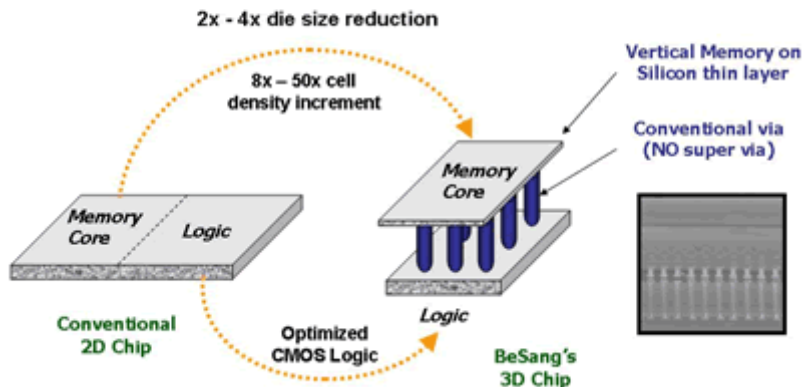
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On August 11, 2008 BeSang, Inc., in collaboration with Korea's National Nanofab Center (NNFC), and Stanford University Nanofab Center (SNF) jointly announced functioning 3D multilayer silicon chips that combine memory and control logic. The unique advantage is unrestricted 3D interconnection using conventional via technology that requires neither wafer alignment nor through-silicon vias.

BeSang creates a second silicon layer of active devices on a single silicon wafer by transferring a submicron-thick silicon device layer from a donor wafer onto a fully processed silicon wafer. The devices combine vertical transistor memory cells layered over CMOS control logic circuitry on a single silicon wafer. **Figure 1** shows the advantages of the layered silicon process over a conventional 2-chip solution.

BeSang's "Single Chip" 3D Solution

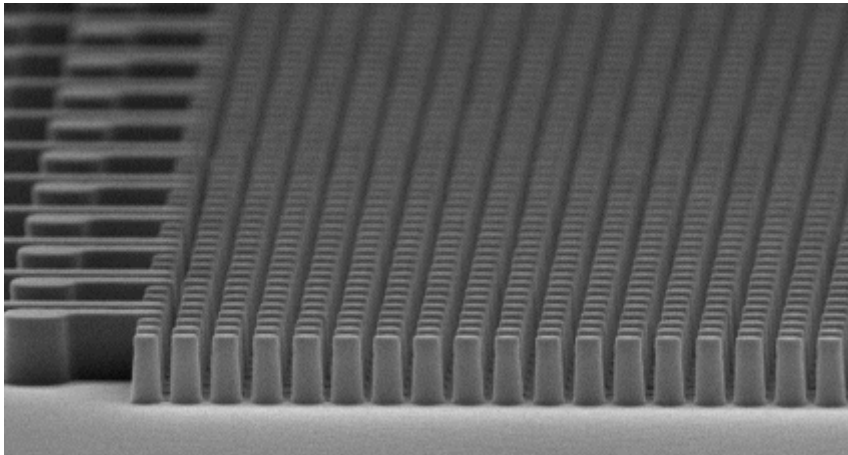
Unlimited *conventional vias* connect memory layer on top of logic circuitry *seamlessly*, which enables high speed "Memory" solutions.



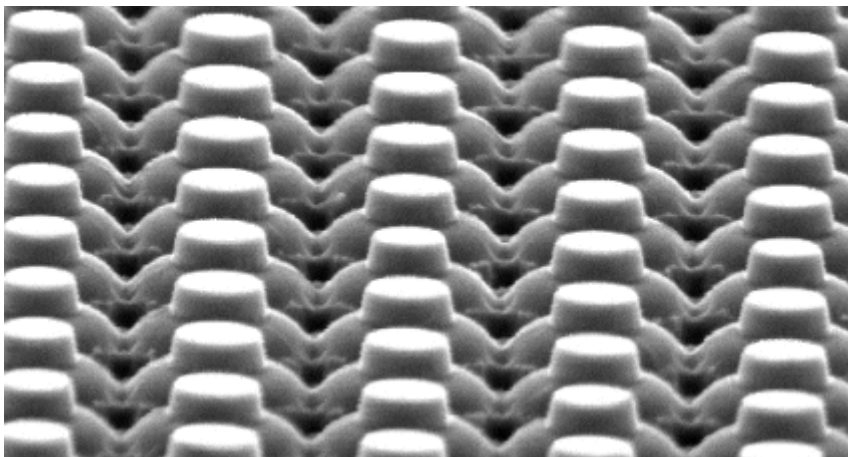
The 8-inch base wafer receives standard 0.18 μ m 950°C CMOS processing to create the control logic. Interconnection and simple via layers are added, and the top surface is planarized to receive the memory layer. The donor silicon wafer is processed at 950°C to form doped layers, creating what is essentially a single large memory cell.

Transferring a thin silicon layer from the donor wafer to the base wafer is a unique process, performed at low temperature (below 400°C) to protect the CMOS devices. The transferred crystalline silicon layer is less than 1µm thick. Since the transferred layer is not yet patterned, alignment tolerances are not stringent.

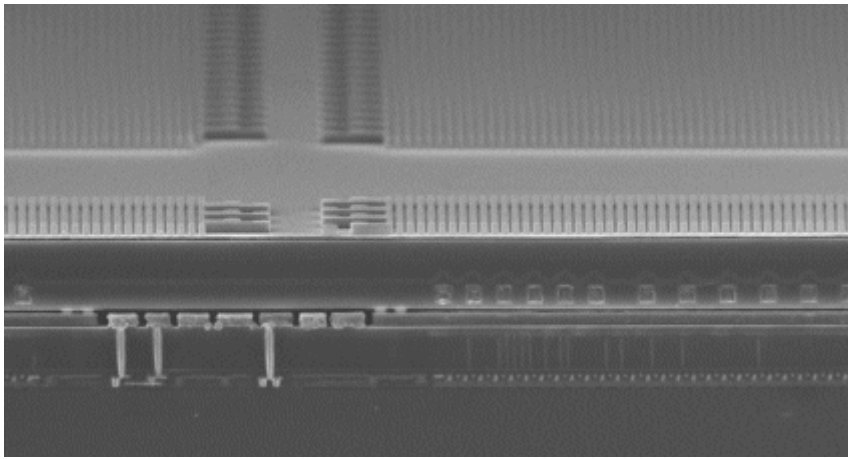
The transferred silicon layer is next patterned and etched into millions of silicon pillars. **Figure 2** shows a part of an array of 0.18µm diameter pillars, just after the pillars are formed.



The array is further processed to make each pillar a surrounded-gate memory cell transistor, with vertically stacked source, gate, and drain. **Figure 3** shows pillars surrounded by gate metallization.



Vias and metal layers complete the interconnections. **Figure 4** is a cross-section of the completed assembly, including the very thin silicon layer on top of the CMOS logic circuits.



The demonstration chips have 128 million vertical transistor memory cells, connected by simple vias to the control logic. The added thickness is negligible, and the transfer process could be repeated to allow unlimited stacking. This high-density Z axis stacking would eliminate the need to increase component density by increase component density by further shrinking of X and Y.

This 3D IC concept was successfully demonstrated by BeSang at SNF in early 2007, and has been further developed with commercial level technologies at NNFC since July 2007. BeSang's 3D IC technology with vertical devices is an innovative, simpler and more cost-effective way to enhance large functional blocks, such as memory arrays or photodiodes for image sensors, systems-on-a-chip, microprocessors, and memory control logic circuitry in advanced semiconductor chips.

FOR MORE INFORMATION

BeSang is a fabless semiconductor company developing its proprietary 3D memory technology. BeSang's high-value intellectual property related to this technology will be useful for companies in the microprocessor, system-on-a-chip, and stand-alone memory markets. For more information, visit the BeSang web site at www.BeSang.com

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