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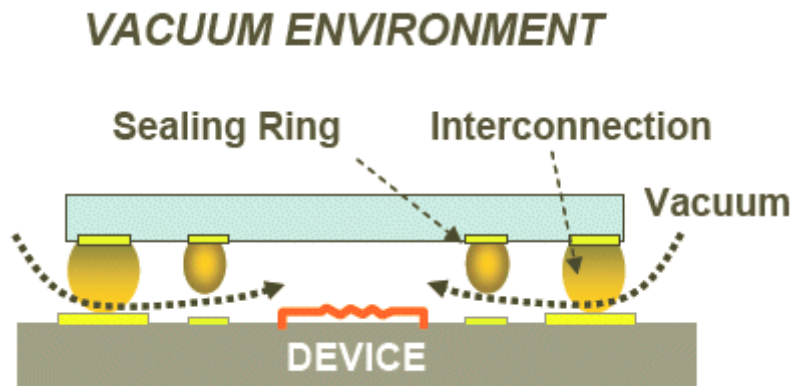
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Chip to Wafer Hermetic Cavity Sealing

George Riley, FlipChips Dot Com

A new application of "controlled collapse" assembly recently reported by SET and CEA-LETI allows fluxless chip to wafer sealing of hermetic cavity devices such as MEMS.

Figure 1 shows the essential features of the patented process. The capping chip solder bump diameter is greater than the height of the seal ring solder. This height differential, as illustrated, holds the cavity open for vacuum or controlled-atmosphere filling before sealing.



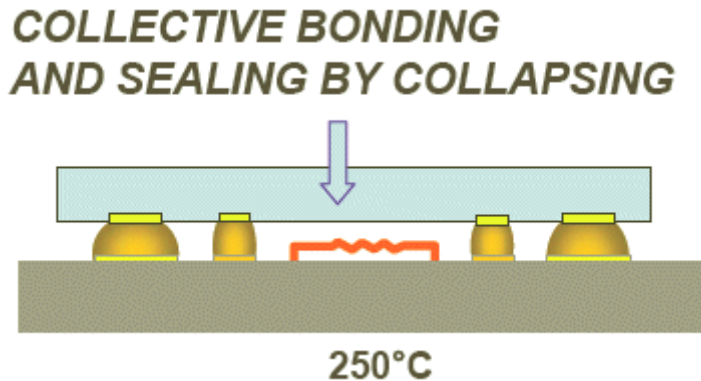
PROCESS

Process steps for fluxless hermetic sealing include:

- Align and tack the chips in place on the surface of the wafer.
- Bring the completely populated wafer under vacuum in the chamber of the specially-modified SET300 aligner-bonder.
- Remove solder surface oxide by introducing oxide-removing gas to the chamber to prepare the Indium bumps and seal ring are for assembly.
- Purge the chamber and return it to vacuum.
- Heat the wafer to collapse the bumps and seal the vacuum cavity.

As the bumps collapse, the surface tension of the molten solder brings all of the chips into optimal X – Y alignment. The wetting pads are designed so that the collapse of the outer bumps lowers the gap enough to bring the seal ring solder into contact with its wetting pad, completing the fluxless solder seal.

Figure 2 shows a single device after ball collapse and sealing.



ADVANTAGES

While chip to wafer assembly has lower throughput than wafer-to-wafer assembly, it offers several offsetting benefits. All of the capping die can be pre-tested and known good. Wafer devices can be pre-tested, to avoid capping unsatisfactory devices. Both of these are yield advantages.

Chip to wafer bonding offers flexibility in both die size and die technology. Wafer-to-wafer assembly requires identical devices of a single technology, and bonds all chips and devices, including bad ones.

Wafer assembly does not offer the self-alignment of chip assembly. Wafer to wafer assembly requires maintaining flatness and XY tolerances over a far greater distance than chip-to-wafer bonding.

In summary, controlled-collapse fluxless hermetic sealing as developed by SET and CEA-LETI promises many commercial advantages.

FOR MORE INFORMATION

Gilbert Lecarpentier*, Jean Stephane Mottet*, François Marion** *Wafer Level Packaging Chip-to-Wafer Approach using Flux Less Soldering and Featuring Hermetic Seal Capability*, IMAPS 4th Annual Conference on Device Packaging, Scottsdale, Arizona March 18, 2008.

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** CEA-LETI Minatec - Grenoble, France

SET FC300 High Force Device Bonder [Information](#)

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