

Wafer-Level Chip Scale Package with Integrated Passives

John MacIntyre, MCSP, Inc.

Wafer-level chip scale packaging (WL-CSP) provides a packaged, protected, testable device little larger than the die itself, without the need to handle and assemble bare die. The CSP is fully testable, and easily handled as a standard surface-mount (SMT) device. CSPs are made in thousands of variations to serve a wide range of applications.

While older and more complex CSP command price premiums, they have limited versatility, and generally require processing on the wafer. Most contain only a single chip, with no integration of other system elements.

To meet this need, MCSP, Inc. has developed a simple wafer-level chip scale package using thin-film wafer processes on a single glass sheet to form chip size packages that require no die-level processing, and can integrate resistor, capacitor, and inductor elements as part of the package. The passive components can be tested and trimmed before the glass substrate is bonded to the wafer.

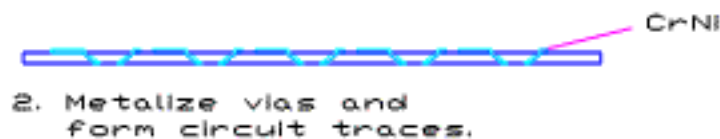
Basic Package

The MCSP package begins with a trimmed wafer-sized sheet of thin (50 to 75 μ m) glass having a thermal expansion coefficient matched to that of the wafer. Vias are created on the glass sheet, matching the die bond pads on the wafer. The glass sheet is coated on the top side with a thin metal film, aligned, and bonded to the wafer. A further metal deposition and patterning brings out connections on the glass in an area-array pattern for easy SMT connection.

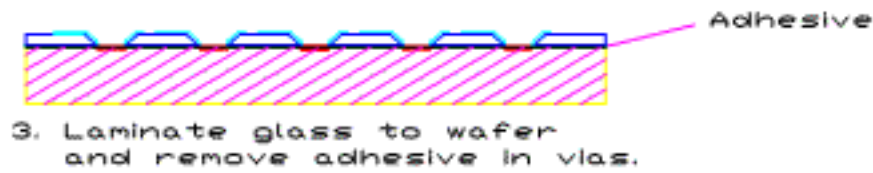
Figure 1 shows the construction steps:



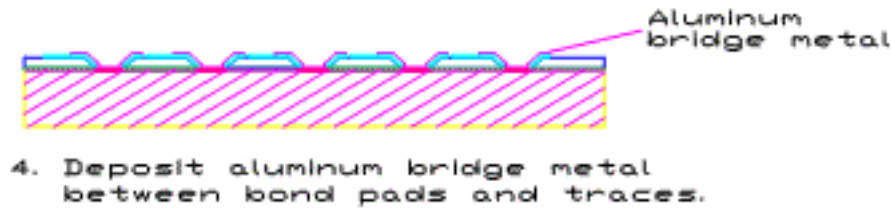
Step 1. The glass sheet is patterned and vias opened by etching or other means. The via taper facilitates uniform metal deposition.



Step 2. The glass sheet is metallized with 500 Å of Cr and 1500-2000 Å of Ni. Following metallization, a photoresist polyimide is applied, exposed and developed to open the Cr-Ni traces and solder pads.



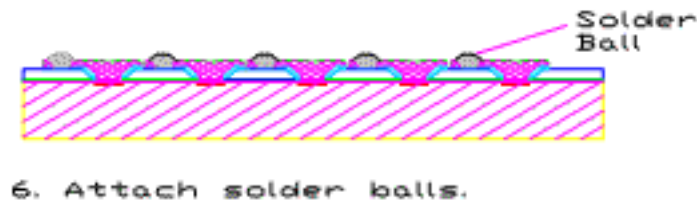
Step 3. The metallized glass sheet/wafer sandwich is formed using an optically transparent adhesive with the wafer after carefully aligning the wafer to the metallized glass sheet.



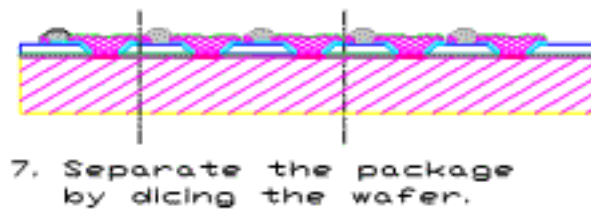
Step 4. Photoresist is again applied to the sandwich to cover the solder pads and open the traces. The traces and vias are cleaned by ashing in a plasma chamber to remove organic materials from the metal surface. The bridge metal layer of aluminum is deposited to link the die bond pads to the traces. Since the die bond pads are aluminum, no pad remetalization or barrier layer is required.



Step 5. After depositing bridge metal, the photoresist and the field metals are removed in a plasma chamber and a non-hydroscopic solder mask is applied to protect the traces around the solder pads. The solder mask is photoimageable and is applied by laminating a sheet or stencil printing a paste. The solder mask is next exposed and developed to open the solder pads for solder attach process.



Step 6. Following, plasma ashing of the solder pads, eutectic solder balls are attached. A conformal coating is sprayed onto the solder ball side of the package for enhanced solder joint reliability.



Step 7. The wafer/glass sandwich is diced to form individual CSPs.

Figure 2 is a cross-sectional view of a portion of the finished package. The blue-colored bridge metal closes the narrow gap opened by the glass and adhesive between the via metal and the die bond pad.

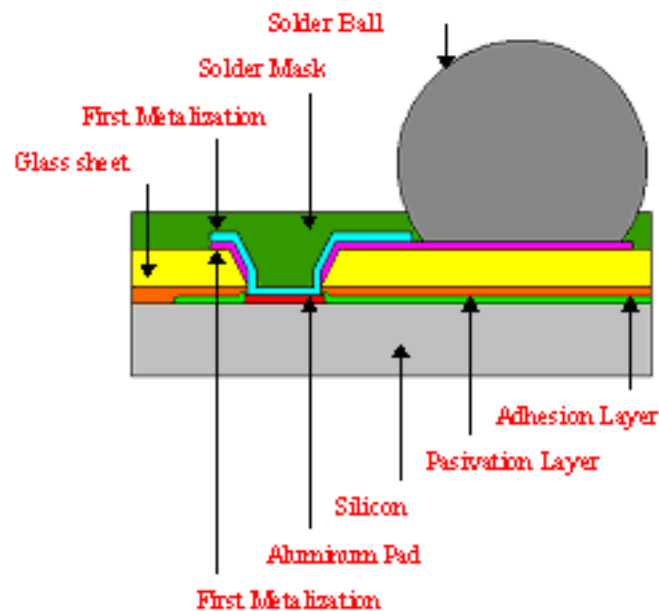


Figure 2. Package cross-section

Package Advantages

The MCSP package uses simple, thin-film processes on top of a protective glass sheet. Via openings and metal are deposited on the glass before bonding to the wafer. This allows inspection and verification before bonding to the wafer, so that discrepancies do not sacrifice expensive wafers. Die shrinks are readily accommodated by shrinking the glass pattern.

The MCSP package requires no costly wafer processing or preparation. The use of a bridge metal eliminates diffusion barriers and chip pad remetalization, so standard wafers can be used unchanged. A fully hermetic version of the package requires only some noble-metal sealing before dicing. The package

can also be configured for 3D stacking.

The package is adaptable to any size die or wafer. Packages can be produced with JEDEC standard outlines and pad layouts. The overall package height is less than 250 μm . The package can be mounted to a board using standard SMT tooling and handling.

Passive Device Integration

The glass sheet can serve as a hybrid substrate, integrating multiple resistor, capacitor, and inductor elements with thin-film interconnections before bonding it to the wafer. This simplifies the design, and enables much greater circuit densities. The shorter in-circuit chip distances reduce interconnection inductance, improving electrical performance. Figure 3 shows a cutaway view of the completed package with integrated passive components.

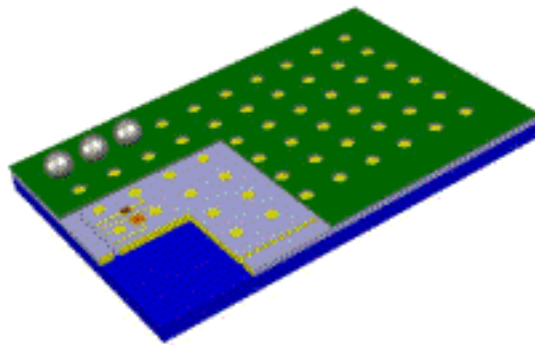


Figure 3. MCSP passive and active device integrated chip-scale package. Passive components are shown mounted on the light blue layer.

Availability

MCSP, Inc. has six issued U.S. patents covering the package structure, the methodology, and the hermetic sealing technique. The company offers licensing under these patents to qualified manufacturers. MCSP, Inc. also offers sub-contractor services for design, fabrication, and testing of the packages, with or without integrated passive devices.

Conclusion

The MCSP wafer-level chip scale package is a low-cost, versatile solution with size, performance and reliability meeting the growing demands of many markets. Integrated passive components allow more compact, higher performance equipment, with lower production costs. Hermeticity suits it to a wide range of environments and applications.

For more information: Visit the company web site at www.microcsp.com