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Quilt Packaging

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"Quilt Packaging" (QP) addresses the need for improved chip input/output performance with a new approach to inter-chip interconnections. QP allows contiguous tiling of ICs in two dimensions with gaps of only a few microns (µ m) between the chips. Quilt Packaging is **promising, fundamentally simple, and practical**.

Advantages include:

- ultrahigh-bandwidth signal transmission between chips.
- lower power dissipation.
- higher silicon efficiency.
- lower system weight and volume.
- potentially improved interconnect reliability.
- lower cost.

Quilt Packaging Structure

QP employs a multitude of short, conductive nodules that protrude horizontally from the vertical sides of IC chips to interconnect with matching nodules on other ICs, resulting in an array of chips that we call a "quilt." These nodules have been fabricated at Notre Dame in widths ranging from 10 to 100 µ m.

Figures 1 and 2 show two examples of nodules "keyed" for self alignment. The keys and slots for a given size of nodule assure correct alignment of the chips in the X-Y plane.

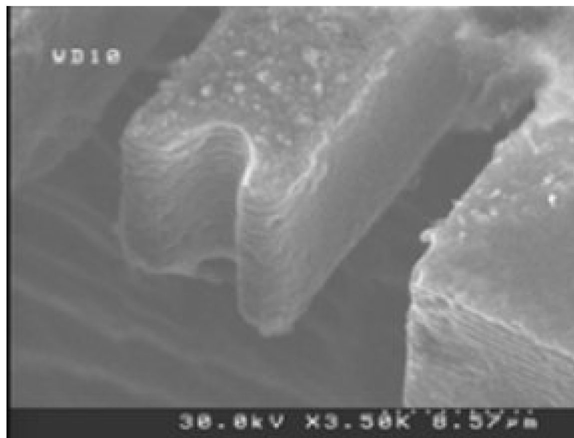


Figure 1. 10 micron slotted nodule on side of die.

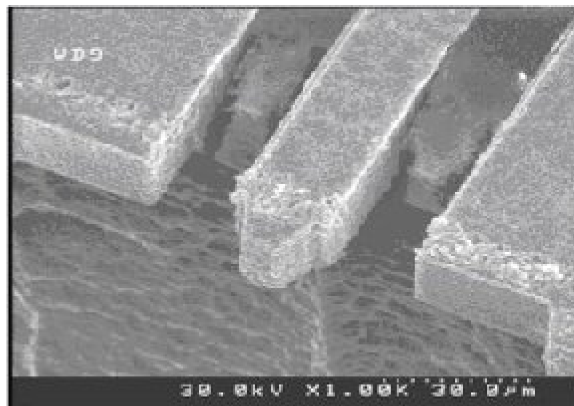


Figure 2. 20 micron keyed nodule on side of die.

Assuming that nodules of at least 5 µm are practical, a 15 mm chip would be able to make up to **1,500 connections per edge** to adjacent die. This could greatly improve system performance while simplifying expensive and power-inefficient, area-inefficient wiring board materials.

Quilt Packaging Fabrication Process

Fabricating QP structures adds two low-resolution photomasks, two deep reactive ion etch (DRIE) steps, dielectric and metal deposition steps, and one chemical-mechanical polishing (CMP) step to the conventional IC fabrication process. The process steps are shown in Figure 3.

Figure 3. Process Steps

Step 1. Define and etch nodules by DRIE.

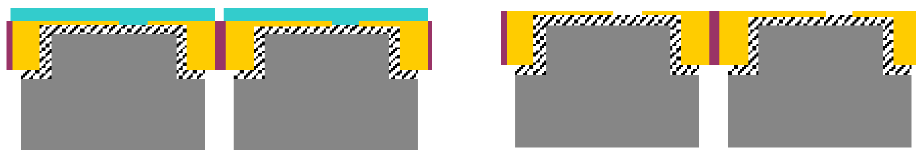
Step 2. Passivate trenches by PECVD SiO_2.

Step 3. Sputter Ti/Cu seed layer inside trenches and plate copper to fill trenches.

Step 4. Planarize the nodules by CMP and continue BEOL processing to finish ICs, making chip I/O connections to the nodules through metalization vias.

Step 5. Spin thick photoresist as protection layer, open separation area and remove SiO_2.

Step 6. Use DRIE to separate the chips.

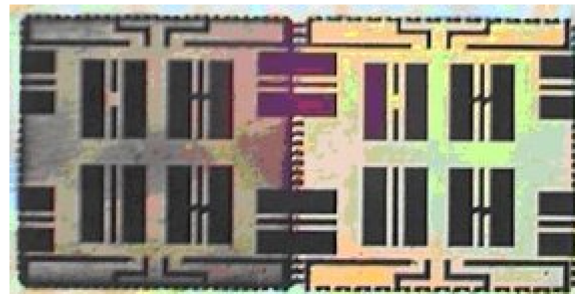


Step 7. Fix the two chips in contact at the nodules, and electrolessly plate Sn at the nodule interfaces.

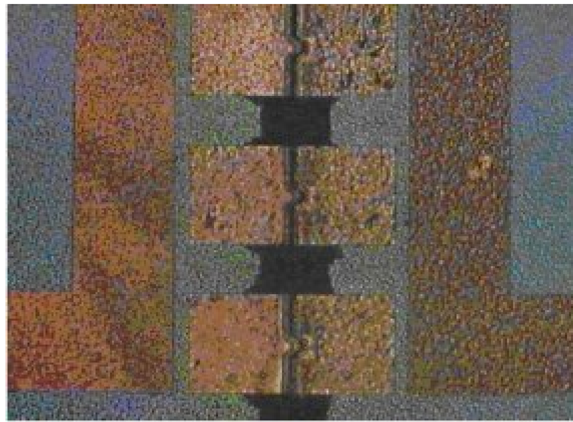
Step 8. Remove photoresist after soldering.

Quilt Packaging Examples

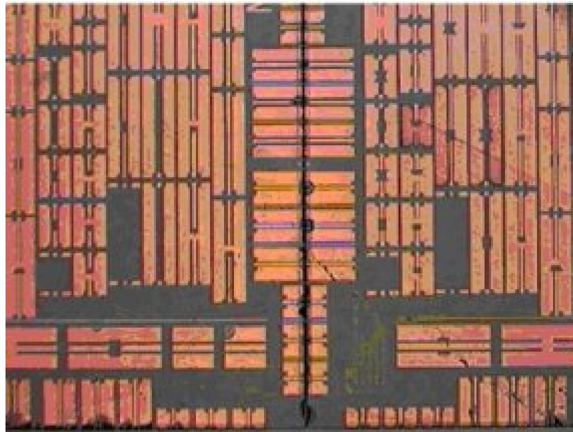
- Figure 4. Two 4-mm chips with coplanar microwave guide test structures configured as a quilt.



- Figure 5. 100-micron nodules self-aligned through keys and slots.



- Figure 6. Two 10mm microwave test chips joined by electrolessly plated tin.



Nodules may be joined in other ways, including reflow of deposited solder, ultrasonic welding, and laser welding. These coplanar waveguide structures are typical of those used to test the microwave performance of the technology.

Electrical Performance

A process for Quilt Packaging of two-die quilts has been developed and demonstration devices have been tested, with RF measurements of electrical performance up to 40 GHz.

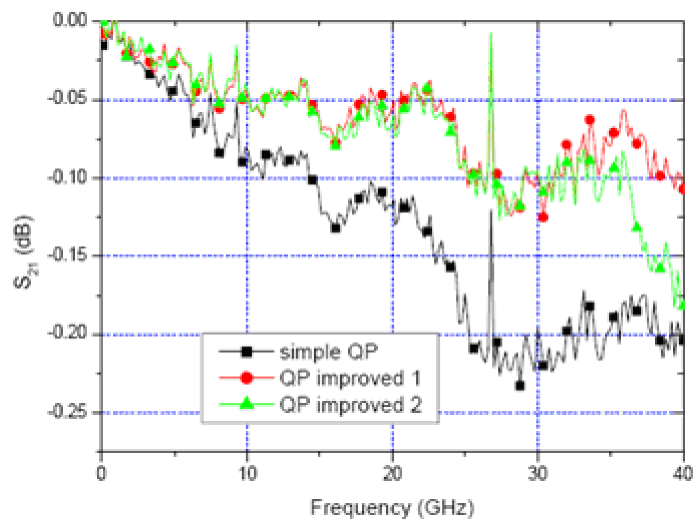


Figure 7. RF performance of some QP designs.

The results shown in Figure 7 are extremely promising. Insertion losses measured as lower than **0.1 dB at up to 40 GHz** for certain nodule designs on high-resistivity silicon substrates.

These results have important implications for the development of advanced RF and digital systems including high performance computing applications:

- QP offers an increase in interchip communications bandwidth of at least 10X, and perhaps up to 100X, over conventional technology.
- New architectures with memory contiguous to processors will allow latency of data access to be reduced.
- Multicore processing quilts will make possible designs more powerful than anything fabricated on a single chip.
- Use of heterogeneous manufacturing technologies or materials will optimize performance. For example III-V optical interconnect controllers may be contiguous with processors.
- QP benefits may be extended to space, satellite systems, and other national security applications.

Continuing QP Development

At Notre Dame, we are developing Quilt Packaging for advanced computing systems in four areas:

- Architectures for both digital processing and pattern recognition chips.
- Basic manufacturing and reliability.
- Demonstrations of quilted silicon CMOS circuits.
- RF performance improvements.

We predict that **within two years**, **QP will be ready for industry to begin incorporating these new topologies into commercial systems**, starting with two-chip quilts in the most critical data processing paths, and leading eventually to fully-quilted systems for revolutionary new applications.

FOR MORE INFORMATION

Publications:

G. H. Bernstein, Q. Liu, M. Yan, Z. Sun, W. Porod, G. Snider, and P. Fay, "Quilt Packaging: High-Density, High-Speed Interchip Communications," IEEE Trans. Adv. Packaging, in press.

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Q. Liu, P. Fay, and G. H. Bernstein, "A Novel Scheme for Wide Bandwidth Chip-to-Chip Communications," J. Microelectronics and Electronics Packaging, vol. 4(1), pp. 1-7 (2007).

G. H. Bernstein, Q. Liu, Z. Sun, and P. Fay, "Quilt Packaging: A New Paradigm for System-in-Package," Proceedings of the IEEE 7th Electronics Packaging Technology Conference (EPTC2005), pp. 1-6, (2005).

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