

Technical Papers in SET Technical Bulletin *“Die Bonding Applications.”*

“An Innovative Die to Wafer 3D Integration Scheme: Die to Wafer Oxide or Copper Direct Bonding with Planarised Oxide Inter-Die Filling”, L. Di Cioccio^{a*}, P. Gueguen^a, L. Clavelier^a, T. Signamarcheix^a, L. Bally^a, L. Vandroux^a, M. Zussy^a, S. Verrun^a, J. Dechamp^a, P. Leduc^a, M. Assous^a, D. Bouchu^a, F. de Crecy^a, L-L. Chapelon^b, R. Taibi^b, ^aCEA/Leti-Minatec, ^bSTMicroelectronics, IEEE 3DIC 2009.

“RF MEMS and Flip-Chip for Space Flight Demonstrator”, C. Drevon, O. Vendier, A. Renel, Thales Alenia Space.

“Electrically Yielding Collective Hybrid Bonding for 3D Stacking of ICs”, A. Jourdain, P. Soussan, B. Swinnen, E. Beyne, IMEC, ECTC 2009.

“A Fluxless Bonding Process using AuSn or Indium for a Miniaturized Hermetic Package”, M. Volpert¹, C. Kopp¹, J. Routin¹, A. Gasse¹, S. Bernabe¹, C. Rossat², M. Tournair², R. Hamelin², V. Lecocq², ¹CEA-LETI-MINATEC, ²INTEXYS PHOTONICS, ECTC 2009.

“High Density Cu-Sn TLP Bonding for 3D Integration”, R. Agarwal, W. Zhang, P. Limaye, W. Ruythooren, IMEC, ECTC 2009.

“Three Dimensional Interconnects with High Aspect Ratio TSVs and Fine Pitch Solder Microbumps”, A. Yu¹, J.H. Lau², S. W. Ho¹, A. Kumar¹, Hnin Wai Yin¹, Jong Ming Ching¹, Vaidyanathan Kripesh¹, D. Pinjala¹, S. Chen³, C-F. Chan³, C-C. Chao³, C-H Chiu³, C-M Huang³, C. Chen³, ¹ Institute of Microelectronics - A*STAR, ² Department of Mechanical Engineering - Hong Kong University Science & Technology, ³ Siliconware Precision Industries Co. Ltd, ECTC 2009.

“High Density Cu-Cu Interconnect Bonding for 3-D Integration”, J. Lannon Jr., C. Gregory, M. Lueck, A. Huffman, D. Temple, RTI International, ECTC 2009.

“Manufacturing & Stacking of Ultra-Thin Film Packages”, Y-C. Shih, T-Y. Kuo, Y-P. Hung, J-Y. Chang, C-Y. Cheng, K-C. Chen, C-K. Lee, C-K. Hsu, J-H. Huang, Z-C. Hsiao, C-T. Ko, Y-H. Chen, Industrial Technology Research Institute (ITRI), ECTC 2009.

“New Reflow Soldering and Tip in Buried Box (TB2) Techniques for Ultrafine Pitch Megapixels Imaging Array”, D. Saint-Patrice, F. Marion, M. Fendler, G. Dumont, J. Garrione, C. Largeron, H. Ribot, F. Greco, M. Diop**, V. Mandrillon*, CEA – LETI, MINATEC, *CEA – LETI, MINATEC localized at ** Ecole Nationale Supérieur des Mines de Saint-Etienne, ECTC 2008.

“Electrical Characterization of High Count, 10 µm Pitch, Room-Temperature Vertical Interconnections”, F. Marion*, D. Saint Patrice*, M. Fendler*, F. Berger*, H. Ribot*, G. Lecarpentier**, J. Macheda**, * CEA-LETI-MINATEC, ** SET S.A.S., Imaps Device Packaging 2009.

“3D Stacked Chip Technology Using Bottom-up Electroplated TSVs”, H. H. Chang^{1,2}, Y. C. Shih¹, Z. C. Hsiao¹, C. W. Chiang¹, Y. H. Chen¹, K. N. Chiang², ITRI¹, Department of Power Mechanical Engineering, National Tsing Hua University², ECTC 2009.

“Study of 15µm Pitch Solder Microbumps for 3D-IC Integration”, A. Yu¹, J. H. Lau², S. Wee Ho¹, A. Kumar¹, W. Yin Hnin¹, D-Q. Yu¹, M. Ching Jong¹, V. Kripesh¹, D. Pinjala¹, D-L. Kwong¹, ¹ Institute of Microelectronics-A*STAR, ² Department of Mechanical Engineering-Hong Kong University Science & Technology.

3D Stacked IC Demonstration using a Through Silicon Via First, J. Van Olmen, A. Mercha, G. Katti¹, C. Huyghebaert, J. Van Aelst, E. Seppala, Zhao Chao, S. Armini, J. Vaes, R. Teixeira Cotrin, M. Van Cauwenberghe, P. Verdonck, K. Verhemeldonck, A. Jourdain, W. Ruythooren, M. de Potter de ten Broeck, A. Opdebeeck, T. Chiarella, B. Parvais, I. Debusschere, T.Y. Hoffmann, M. Stucchi, M. Rakowski, Ph. Soussan, R. Cartuyvels, E. Beyne, S. Biesemans, B. Swinnen, W. Dehaene¹, IMEC, ¹ EE Department-K.U. Leuven.